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10/799,193	03/12/2004	Hiromitsu Yamaguchi	1232-5326	8180

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EXAMINER	
GOLDBERG, BRIAN J	
ART UNIT	PAPER NUMBER
2861	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,193	YAMAGUCHI ET AL.	
	Examiner	Art Unit	
	Brian Goldberg	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1 and 3-17 are objected to because of the following informalities:

2. Regarding claim 1, the claim recites the limitations "the first print elements" in line 6 of the claim, "the end of the chip" in line 7 of the claim, "the number of second print elements" in line 13 of the claim, and "the plurality of drive blocks in line 17 of the claim. There is insufficient antecedent basis for these limitations in the claim. Furthermore, "the end of the chip" in line 7 should be changed to "the end of the chips" to maintain consistency in the claim. Appropriate correction is required.

3. Regarding claim 6, the claim recites the limitations "the first print elements" in line 7 of the claim, "the end of the chip" in lines 7-8 of the claim, and "the number of second print elements" in line 17 of the claim. There is insufficient antecedent basis for these limitations in the claim. Furthermore, "the end of the chip" in lines 7-8 should be changed to "the end of the chips" to maintain consistency in the claim. Appropriate correction is required.

4. Regarding claim 11, the claim recites the limitations "the first print elements" in line 6 of the claim, "the end of the chip" in line 6 of the claim, and "the number of second print elements" in line 17 of the claim. There is insufficient antecedent basis for these limitations in the claim. Furthermore, "the end of the chip" in line 6 should be changed to "the end of the chips" to maintain consistency in the claim. Appropriate correction is required.

5. Regarding claim 16, the claim recites the limitations "the first print elements" in line 6 of the claim, and "the end of the chip" in lines 6-7 of the claim. There is insufficient antecedent basis for these limitations in the claim. Furthermore, "the end of the chip" in lines 6-7 should be changed to "the end of the chips" to maintain consistency in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6, 8-11, and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano et al. (US 6352327) in view of Ikemoto et al. (US 6598951).

8. Regarding claim 6, Yano et al. disclose "a print head (5 of Fig 2) having a plurality of arrayed chips (5a-5d of Fig 1, col 14 ln 39-43), the chips each having a plurality of print elements arranged in a column direction (see Fig 3, N1, Ni, N64) the plurality of print elements being divided in a number of time-division drive blocks (col 7 ln 54-66), ... the print head and a print medium are moved relative to each other in a scan direction that crosses the column direction (A and B of Fig 1); the plurality of print elements of each of said drive blocks are activated in the drive blocks on a time-division basis to form an image on the print medium (col 7 ln 54-66); ... and the number of second print elements in the adjoining chips aligned in the scan direction is equal to an integer times the number of time-division drive blocks (col 6 ln 61-65, col 7 ln 62-66)."

Thus Yano et al. meet the claimed invention except "the plurality of print elements including the first print elements and at least two second print elements situated near the end of the chip in relation to the first print elements... the first print elements in adjoining chips are not aligned in the scan direction; the second print elements in adjoining chips are aligned in the scan direction with printing positions which overlap in the scan direction."

9. Ikemoto et al. teach "the plurality of print elements including the first print elements (for example, 4, 5, 6 of Fig 17) and at least two second print elements situated near the end of the chip in relation to the first print elements (for example, 1, 2, 3 of Fig 17)... the first print elements in adjoining chips are not aligned in the scan direction (see 4, 5, 6 of Fig 17); the second print elements in adjoining chips are aligned in the scan direction with printing positions which overlap in the scan direction (see overlap portions of Fig 17)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to arrange the chips of Yano et al. in a way described by Ikemoto et al. One would have been motivated to so modify Yano et al. for the benefit of providing a head arrangement with a lower cost of manufacturing while maintaining high resolution and image quality, as well as reduced power consumption, as stated by Ikemoto et al.

10. Regarding claim 8, Yano et al. disclose "the plurality of print elements in the print head are arranged in an entire widthwise printable range of the print medium (col 14 ln 32-38)."

11. Regarding claim 9, Yano et al. disclose "the plurality of print elements in the print head are ink jet print elements that can be activated to eject ink from nozzles (col 2 ln 66-67, col 6 ln 4-6)."

12. Regarding claim 10, Yano et al. disclose "the ink jet print elements have electrothermal transducers that generate energy for ejecting ink (col 13 ln 49-53)."

13. Regarding claim 11, a plurality of arrayed chips (5a-5d of Fig 1, col 14 ln 39-43), the chips each having a plurality of print elements arranged in a column direction (see Fig 3, N1, Ni, N64) the plurality of print elements being divided in a number of time-division drive blocks (col 7 ln 54-66), ... the print head and a print medium are moved relative to each other in a scan direction that crosses the column direction (A and B of Fig 1); the plurality of print elements of each of the drive blocks are activated in the drive blocks on a time-division basis to form an image on the print medium (col 7 ln 54-66); ... the number of second print elements in the adjoining chips aligned in the scan direction is equal to an integer times the number of time-division drive blocks (col 6 ln 61-65, col 7 ln 62-66)." Thus Yano et al. meet the claimed invention except "the plurality of print elements including the first print elements and at least two second print elements situated near the end of the chip in relation to the first print elements... the first print elements in adjoining chips are not aligned in the scan direction; the second print elements in adjoining chips are aligned in the scan direction with printing positions which overlap in the scan direction forming a set of print elements."

14. Ikemoto et al. teach "the plurality of print elements including the first print elements (for example, 4, 5, 6 of Fig 17) and at least two second print elements situated

near the end of the chip in relation to the first print elements (for example, 1, 2, 3 of Fig 17)... the first print elements in adjoining chips are not aligned in the scan direction (see 4, 5, 6 of Fig 17); the second print elements in adjoining chips are aligned in the scan direction with printing positions which overlap in the scan direction forming a set of print elements (see overlap portions of Fig 17)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to arrange the chips of Yano et al. in a way described by Ikemoto et al. One would have been motivated to so modify Yano et al. for the benefit of providing a head arrangement with a lower cost of manufacturing while maintaining high resolution and image quality, as well as reduced power consumption, as stated by Ikemoto et al.

15. Regarding claim 13, Yano et al. disclose "the plurality of print elements in the print head are arranged in an entire widthwise printable range of the print medium (col 14 ln 32-38)."

16. Regarding claim 14, Yano et al. disclose "the plurality of print elements in the print head are ink jet print elements that can be activated to eject ink from nozzles (col 2 ln 66-67, col 6 ln 4-6)."

17. Regarding claim 15, Yano et al. disclose "the ink jet print elements have electrothermal transducers that generate energy for ejecting ink (col 13 ln 49-53)."

18. Claims 1, 3-5, 7, 12, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano et al. (US 6352327) in view of Ikemoto et al. (US 6598951) and further in view of Takagi et al. (US 6217149).

19. Regarding claim 1, Yano et al. disclose "a print head (5 of Fig 2) has a plurality of arrayed chips (5a-5d of Fig 1, col 14 ln 39-43), the chips each have a plurality of print elements arranged in a column direction (see Fig 3, N1, Ni, N64 and 64 nozzles of Fig 6C) the plurality of print elements are divided in a number of time-division drive blocks (col 7 ln 54-66)...the number of second print elements is equal in number to an integer times the number of time-division drive blocks (col 9 ln 47-54)...moving the print head (5 of Fig 2) and a print medium (1 of Fig 1) relative to each other in the scan direction (A and B of Fig 1) that crosses the column direction; and dividing the first print elements into the plurality of drive blocks and activating the drive blocks of the first print elements on a time-division basis to form an image on the print medium (col 7 ln 54-66)." Thus Yano et al. meet the claimed invention except "the plurality of print elements include the first print elements and at least two second print elements situated near the end of the chip in relation to the first print elements, and the chips are arranged so that the second print elements in adjoining chips are aligned in a scan direction with printing positions which overlap in the scan direction; wherein the chips are arranged so that the first print elements in adjoining chips are not aligned in the scan direction" and "wherein drive timings with which to activate the set of print elements aligned in the scan direction have the same time-division drive timing."

20. Ikemoto et al. teach "the plurality of print elements include the first print elements (for example, 4, 5, 6 of Fig 17) and at least two second print elements (for example, 1, 2, 3 of Fig 17) situated near the end of the chip in relation to the first print elements, and the chips are arranged so that the second print elements in adjoining chips are aligned

in a scan direction with printing positions which overlap in the scan direction (see overlap portions of Fig 17); wherein the chips are arranged so that the first print elements in adjoining chips are not aligned in the scan direction (see 4, 5, 6 of Fig 17)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to arrange the chips of Yano et al. in a way described by Ikemoto et al. One would have been motivated to so modify Yano et al. for the benefit of providing a head arrangement with a lower cost of manufacturing while maintaining high resolution and image quality, as well as reduced power consumption, as stated by Ikemoto et al.

21. Takagi et al. teach "wherein drive timings with which to activate the set of print elements aligned in the scan direction have the same time-division drive timing (col 8 ln 25-55, Fig 8A)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to drive printing elements aligned in the scan direction at the same time. One would have been motivated to so modify Yano et al. in view of Ikemoto et al. for the benefit of forming a plurality of dots that are aligned in the sub-scanning direction using a set of print elements aligned in the scan direction, regardless of the nozzle arrangement, as stated by Takagi et al.

22. Regarding claim 3, Yano et al. further disclose "the plurality of print elements in the print head are arranged in an entire widthwise printable range of the print medium (col 14 ln 32-38)."

23. Regarding claim 4, Yano et al. further disclose "the plurality of print elements in the print head are ink jet print elements that can be activated to eject ink from nozzles (col 2 ln 66-67, col 6 ln 4-6)."

24. Regarding claim 5, Yano et al. further disclose "the ink jet print elements have electrothermal transducers that generate energy for ejecting ink (col 13 ln 49-53)."

25. Regarding claims 7 and 12, Yaho et al. in view of Ikemoto et al. disclose the claimed invention as set forth above regarding claims 6 and 11 respectively. Thus Yano et al. meet the claimed invention except "the print elements aligned in the scan direction are allocated to the same drive block for activation."

26. Takagi et al. teach "the print elements aligned in the scan direction are allocated to the same drive block for activation (col 8 ln 25-55, Fig 8A)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to drive printing elements aligned in the scan direction at the same time. One would have been motivated to so modify Yano et al. in view of Ikemoto et al. for the benefit of forming a plurality of dots that are aligned in the sub-scanning direction using a set of print elements aligned in the scan direction, regardless of the nozzle arrangement, as stated by Takagi et al.

27. Regarding claim 16, Yano et al. disclose "a print head (5 of Fig 2) has a plurality of arrayed chips (5a-5d of Fig 1, col 14 ln 39-43), the chips each have a plurality of print elements arranged in a column direction (see Fig 3, N1, Ni, N64 and 64 nozzles of Fig 6C) the print elements arranged are divided in a number of time-division drive blocks (col 7 ln 54-66)...moving the print head (5 of Fig 2) and a print medium (1 of Fig 1) relative to each other in the scan direction (A and B of Fig 1) that crosses the column direction; activating the drive blocks of the plurality of print elements on a time-division basis to form an image on the print medium (col 7 ln 54-66)." Thus Yano et al. meet the

claimed invention except "the plurality of print elements include the first print elements and at least two second print elements situated near the end of the chip in relation to the first print elements, and the chips are arranged so that the second print elements in adjoining chips are aligned in a scan direction with printing positions which overlap in the scan direction; wherein the chips are arranged so that the first print elements in adjoining chips are not aligned in the scan direction" and "activating the second print elements at the same time-division drive timing."

28. Ikemoto et al. teach "the plurality of print elements include the first print elements (for example, 4, 5, 6 of Fig 17) and at least two second print elements (for example, 1, 2, 3 of Fig 17) situated near the end of the chip in relation to the first print elements, and the chips are arranged so that the second print elements in adjoining chips are aligned in a scan direction with printing positions which overlap in the scan direction (see overlap portions of Fig 17)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to arrange the chips of Yano et al. in a way described by Ikemoto et al. One would have been motivated to so modify Yano et al. for the benefit of providing a head arrangement with a lower cost of manufacturing while maintaining high resolution and image quality, as well as reduced power consumption, as stated by Ikemoto et al.

29. Takagi et al. teach "activating the set of print elements aligned in the scan direction at the same time-division drive timing (col 8 ln 25-55, Fig 8A)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to drive printing elements aligned in the scan direction at the same time. One would have

been motivated to so modify Yano et al. in view of Ikemoto et al. for the benefit of forming a plurality of dots that are aligned in the sub-scanning direction using a set of print elements aligned in the scan direction, regardless of the nozzle arrangement, as stated by Takagi et al.

30. Regarding claim 17, Yano et al. further disclose "a storage media readable by a computer and storing the program of claim 16 (20b,c of Fig 2, col 6 ln 30-34, col 15 ln 30-37)."

Response to Arguments

31. Applicant's arguments with respect to claims 1 and 3-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

32. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Goldberg whose telephone number is 571-272-2728. The examiner can normally be reached on Monday through Friday, 9AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Luu can be reached on 571-272-7663. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brian Goldberg BG
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May 7, 2007

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